Applicants have amended claims 1 and 15, the only independent claims, to more clearly define and distinctly claim their invention. After entry of this Amendment and Response, claims 1, 3-12, 15, and 17-27 will be pending in the application. Applicants respectfully traverse the outstanding rejections and request reconsideration and withdrawal of all grounds of pending objections and rejections for the reasons discussed below.

Objections to Drawings

The Office Action objects to the drawings under 37 C.F.R 1.83(a), indicating that every features of claims 1 and 15, specifically pMOSFET and nMOSFET of claim 1, and n-channel transistor and p-channel transistor of claim 15 must be shown in the drawings. Applicants respectfully submit that these features are properly shown in FIGS. 4 and 5A, as originally filed.

Specifically, a pMOS transistor and an nMOS transistor are shown in FIG. 4 as elements 402 and 408 respectively. A generic MOSFET, which can be either a pMOSFET or an nMOSFET, is shown in FIG. 5A. As one skilled in the art would recognize, p- and n-type MOSFETS are defined by the type of electrical conduction that depends on n and p doping levels of the heterostructure. Thus, the generic MOSFET shown in FIG. 5A depicts both a pMOSFET and an nMOSFET. Likewise, the "Strained-Si High Mobility Channel" shown in FIG. 5A as element 508 can either be a p-channel transistor or an n-channel transistor depending on the doping of the heterostructure. Thus, Applicants respectfully submit that all features of claims 1 and 15 are shown in the drawings and request reconsideration and withdrawal of the objection under 37 C.F.R. 1.83(a).

Objections to the Claims

The Office Action objects to claims 8 and 10 for reciting the phrase "bulk silicon" and requires that this phrase be replaced with "substrate." Applicants respectfully disagree. Claims 8 and 10 recite a value for a ratio of gate width of the pMOSFET to the gate width of the nMOSFET. This value equals either the ratio of the electron mobility and hole mobility (claim 8) or the square root of the ratio of the electron mobility and hole mobility (claim 10) of a particular material, i.e. bulk silicon. While Applicants recognize that the substrate recited claims 1 and 15 comprises silicon, Applicants have chosen to define the ratio of gate widths of pMOSFET to nMOSFET in relation to the properties of a specific material, i.e., bulk silicon, and

not with relation to the substrate. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw the objection to claims 8 and 10.

The Office Action also objects to claim 15 and requires Applicants to replace "n transistor" with "n-channel transistor" and a "p transistor" with a "p-channel transistor." Applicants have amended claim 15 accordingly, and request withdrawal of the objection.

Rejections Under 35 U.S.C. §112

The Office Action rejects claims 13 and 14 under 35 U.S.C. § 112, second paragraph as being indefinite. Applicants have cancelled claims 13 and 14, thereby rendering this rejection moot.

Rejections Under 35 U.S.C. §102

Claims 1, 2, 4, 6, 12, 15, 16, 18, 20, 26, and 27 stand rejected under 35 U.S.C. §102(e) as allegedly anticipated by Lustig. Applicants respectfully traverse this rejection to the extent it is maintained over the claims as amended, and submit that Lustig fails to teach or suggest every limitation of independent claims 1 and 15, or claims dependent either directly or indirectly therefrom.

Specifically, claims 1 and 15 recite, in part, a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on the substrate, and a strained surface layer on the relaxed $Si_{1-x}Ge_x$ layer. The heterostructure also includes a planarized surface positioned between the strained surface layer and the Si substrate.

As explained on page 8, line 14 to page 9, line 10 of Applicants' specification, the material quality of relaxed SiGe on Si being insufficient for utilization in CMOS fabrication is a problem well known in the art. During epitaxial growth, the surface of the SiGe becomes very rough as the material is relaxed via dislocation introduction. Applicants disclose that the typical roughness of a grown $Si_{0.8}Ge_{0.2}$ layer is approximately 7.9 nm and this surface roughness typically increases with increasing Ge content of the SiGe layer. Surface roughness of such magnitudes is undesirable for producing CMOS and other electronic devices. Thus, planarization to reduce excessive surface roughness is critical in the production of strained Si devices because it increases the yield for fine-line lithography. Thus, an important feature of the

Applicants' invention is to include a planarized surface, i.e., a layer that has been smoothed, between the Si substrate and the strained surface layer.

Applicants respectfully submit that Lustig does not, as the Examiner contends, disclose a planarized surface positioned between the strained surface layer and the Si substrate. Instead, Lustig merely depicts layers in FIGS. 1-9 that are "planar", i.e. two-dimensional. This is, however, not the same as, or suggestive of, a "planarized" layer whose surface is smoothed.

Specifically, Lustig discloses growing $Si_{1-x}Ge_x$ layers and a strained Si layer on top of the $Si_{1-x}Ge_x$ layers by selective epitaxy. See Lustig, col. 3, lines 54-67 and column 4, lines 1-15. Lustig fails, however, to teach or suggest including a planarized surface, i.e., a layer that has been smoothed, within his device to reduce surface roughness. Thus, Lustig fails to teach or suggest including a planarized surface between the Si substrate and the strained surface layer, as required by claims 1 and 15, as amended. Because Lustig fails to teach all of the elements of Applicants' independent claims 1 and 15, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of independent claims 1 and 15 under 35 U.S.C. § 102(e) based on that reference. Because claims 4, 6, 12, 18, 20, 26, and 27 depend directly or indirectly from independent claim 1 and 15 and recite further limitations thereon, Applicants also request that the Examiner reconsider and withdraw any rejection of these claims based on Lustig.

Rejections Under 35 U.S.C §103(a)

The Office Action rejects claims 3, 7-11, 17, and 21 under 35 U.S.C. § 103(a) as unpatentable over Lustig. The Office Action further rejects claims 5 and 19 under 35 U.S.C. § 103(a) as being unpatentable over Lustig in view of Chu and claims 13, 14, and 22-25 under 35 U.S.C. § 103(a) as being unpatentable over Lustig in view of Kant.

Applicants respectfully traverse this rejection for the reasons described above because Lustig fails to teach or suggest each and every element of Applicants' independent claims 1 and 15. Because claims 3, 5, 7-11, 17, 19, and 21-25 depend directly or indirectly from the allowable base claims 1 and 15 and recite further limitations thereon, Applicants request that the Examiner reconsider and withdraw any rejection of these claims.

Also, Applicants respectfully submit that Chu and/or Kant fails to cure the deficiencies of Lustig. Briefly, Chu teaches a method for forming strained layers on an insulator. See Chu, col. 1, lines 61-67 and column 2, lines 1-7. Kant teaches a method for a reduction in silicon area in

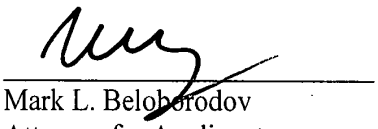
applications where a number of input signals simultaneously transition to the same logic state. See Kant, col. 2, lines 48-50. Neither Chu nor Kant, alone or in combination, teach or suggest a heterostructure including a planarized surface positioned between a strained surface layer and a Si substrate, as recited in Applicants' claims 1 and 15. Thus, Applicants respectfully submit that claims 1 and 15, and all claims depending directly or indirectly therefrom are properly patentable over a combination of Lustig, Chu, and Kant.

CONCLUSION

In view of the foregoing, Applicants respectfully submit that claims 1, 3-12, 15, and 17-27 are novel, non-obvious and are in condition for allowance.

If, in the Examiner's opinion, a telephonic interview would serve to clarify issues and expedite the prosecution of the present application, the undersigned attorney would welcome the opportunity to discuss any outstanding issues, and to work with the Examiner toward placing the application in condition for allowance.

Respectfully submitted,



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COMPLETE LISTING OF ALL PENDING CLAIMS

1. (Currently Amended) A CMOS inverter comprising:

a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer, the heterostructure further including a planarized surface positioned between the strained surface layer and the Si substrate; and

a pMOSFET and an nMOSFET, wherein the channel of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer.

2. (Cancelled)

3. (Original) The CMOS inverter of claim 1, wherein the surface roughness of the strained surface layer is less than 1nm.

4. (Original) The CMOS inverter of claim 1, wherein the heterostructure further comprises an oxide layer positioned between the relaxed Si1-xGex layer and the Si substrate.

5. (Original) The CMOS inverter of claim 1, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed Si1-xGex layer and the Si substrate.

6. (Original) The CMOS inverter of claim 1, wherein the strained surface layer comprises Si.

7. (Original) The CMOS inverter of claim 1, wherein $0.1<x<0.5$.

8. (Original) The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in bulk silicon.

9. (Original) The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the ratio of the electron mobility and the hole mobility in the strained surface layer.

10. (Original) The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in bulk silicon.

11. (Original) The CMOS inverter of claim 7, wherein the ratio of gate width of the pMOSFET to the gate width of the nMOSFET is approximately equal to the square root of the ratio of the electron mobility and the hole mobility in the strained surface layer.

12. (Original) The CMOS inverter of claim 7, wherein the gate drive is reduced to lower power consumption.

13. (Cancelled).

14. (Cancelled).

15. (Currently Amended) An integrated circuit comprising:

a heterostructure including a Si substrate, a relaxed $Si_{1-x}Ge_x$ layer on said Si substrate, and a strained surface layer on said relaxed $Si_{1-x}Ge_x$ layer, the heterostructure further including a planarized surface positioned between the strained surface layer and the Si substrate; and

a p-channel transistor and an n-channel transistor formed in said heterostructure, wherein said strained layer comprises the channel of said n-channel transistor and said p-channel transistor, and said n-channel transistor and said p-channel transistor are interconnected in a CMOS circuit.

16. (Cancelled).

17. (Original) The integrated circuit of claim 15, wherein the surface roughness of the strained layer is less than 1nm.

18. (Original) The integrated circuit of claim 15, wherein the heterostructure further comprises an oxide layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

19. (Original) The integrated circuit of claim 15, wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed $Si_{1-x}Ge_x$ layer and the Si substrate.

20. (Original) The integrated circuit of claim 15, wherein the strained layer comprises Si.

21. (Original) The integrated circuit of claim 15, wherein $0.1<x<0.5$.

22. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises a logic gate.

23. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises a NOR gate.

24. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises an XOR gate.

25. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises a NAND gate.

26. (Original) The integrated circuit of claim 15, wherein the p-channel transistor serves as a pull-up transistor in said CMOS circuit and the n-channel transistor serves as a pull-down transistor in said CMOS circuit.

27. (Original) The integrated circuit of claim 15, wherein the CMOS circuit comprises an inverter.